



(11) EP 1 229 315 A1

(12)

### **EUROPEAN PATENT APPLICATION**

(43) Date of publication: 07.08.2002 Bulletin 2002/32

(51) Int Cl.7: **G01K 7/22**, H01S 5/024

(21) Application number: 02250736.2

(22) Date of filing: 04.02.2002

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 05.02.2001 JP 2001028881

(71) Applicant: Fujitsu Quantum Devices Limited Yamanashi 409-3883 (JP)

(72) Inventor: Kawamura, Hiromitsu, Fujitsu Quantum Devices Ltd. Nakakoma-gun, Yamanashi 409-3883 (JP)

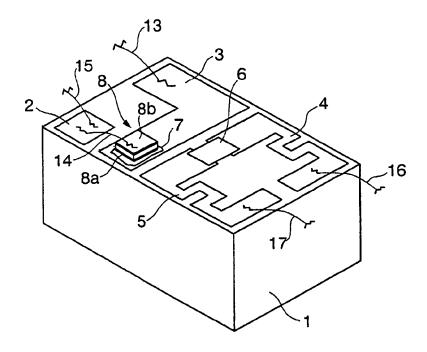
(74) Representative: Fenion, Christine Lesley et al Haseltine Lake & Co., Imperial House, 15-19 Kingsway London WC2B 6UD (GB)

#### (54) Semiconductor device carrier

(57) There is provided a carrier substrate (1), a temperature sensing resistor film (6) formed directly on the carrier substrate (1), first and second conductive patterns (4,5) formed on the carrier substrate (1) and con-

nected to both ends of the temperature sensing resistor film (6) respectively, and a semiconductor chip (8) mounting region portion formed on the carrier substrate (1).

## FIG. 4







[0001] The present invention relates to a semiconductor device and a chip carrier and, more particularly, a structure of a temperature sensor portion of the semiconductor device, for example, a structure of a thermistor element portion employed in temperature control of a laser chip of a semiconductor light emitting device as the major application mode.

[0002] In order to control the temperature of the laser chip in operation, for example, a thermistor is brazed to a ceramic carrier onto which a semiconductor light emitting element, e.g., a laser chip, is mounted, as shown in FIG.1 of the accompanying drawings.

[0003] In FIG.1, a rectangular first conductive pattern 102a and an L-shaped second conductive pattern 102b are formed in a first region that is positioned near one end on a major surface of a ceramic carrier 101. Also, a rectangular third conductive pattern 102c is formed in a second region that is positioned near the other end on the major surface.

[0004] A lower electrode 103a of the laser chip 103 is connected to such second conductive pattern 102b by a conductive brazing material 104, and also a first gold wire 105a is connected to such second conductive pattern 102b by the bonding. Second and third gold wires 105b, 105c that relay the first conductive pattern 102a are electrically connected to an upper electrode 103b of the semiconductor laser 103.

[0005] Also, a thermistor 106 is connected to the third conductive pattern 102c, so that the temperature is sensed in response to change in its resistance.

[0006] The thermistor 106 has first and second electrodes 106b, 106c formed on a major surface of a ceramic substrate 106a, and a thermistor element 106d connected to these first and second electrodes 106b, 106c. The thermistor having such structure is set forth in Patent Application Publication (KOKAI) Hei 6-61012, for example.

[0007] Then, a bottom surface of the ceramic substrate 106a is connected to the third conductive pattern 102c via a solder 107. Also, fourth and fifth gold wires are bonded to the first and second electrodes 106b, 106c respectively and then extended electrically to the outside therefrom. In this case, the third conductive pattern 102c is formed to improve the adhesiveness between the ceramic substrate 106a and the ceramic carrier 101.

[0008] However, in the above structure, the thermal resistance of a solder 107, that is interposed between the ceramic carrier 101 and the thermistor element 106d, changes with time due to the change in microstructure or the progress of crack caused by solder creep after the semiconductor light emitting device is operated.

[0009] Therefore, the resistance value of the thermistor element 106d that is used to sense the temperature of the laser chip 103 changes with the lapse of the time

over which the semiconductor light emitting device is operated.

[0010] Accordingly, it is desirable to provide a semiconductor device and a chip carrier, which is capable of controlling the temperature of a semiconductor chip with high precision.

[0011] According to an embodiment of a first aspect of the present invention, a semiconductor device is provided which comprises a carrier substrate, a temperature sensing resistive element deposited on the carrier substrate, a semiconductor element mounting portion laid on the carrier substrate, and a semiconductor element mounted on the mounting portion.

[0012] In the above semiconductor device, the carrier substrate may be formed of ceramics. Also, conductive patterns may be formed on the carrier substrate that are connected to the temperature sensing resistive element. In this case, each of the conductive patterns may have a bonding point that is electrically connected to an outside, and a portion having low thermal conductivity may be interposed into each of the conductive patterns between the bonding point and the temperature sensing resistive element. The portion having low thermal conductivity may be a bent, and/or small width, portion of each of the conductive patterns.

[0013] In the above semiconductor device, the temperature sensing resistive element may contain at least one of Mn, Ni, Co, and Fe.

[0014] Also, the semiconductor element may be a semiconductor laser. In this case, a heat sink may be interposed between the semiconductor laser and the mounting portion.

**[0015]** According to an embodiment of a second aspect of the present invention a chip carrier is provided which comprises a carrier substrate, a temperature sensing resistive element deposited on the carrier substrate, and a semiconductor element mounting portion laid on the carrier substrate.

[0016] In the above chip carrier, the carrier substrate may be formed of ceramics. Also conductive patterns may be formed on the carrier substrate and connected to the temperature sensing resistive element. In this case, each of the conductive patterns may have a bonding point that is electrically connected to an outside, and a portion having low thermal conductivity may be interposed into each of the conductive patterns between the bonding point and the temperature sensing resistive element. Also, the portion having low thermal conductivity may be a bent, and/or small width, portion of each of the conductive patterns.

[0017] In the above chip carrier, the temperature sensing resistive element may be formed on the carrier substrate by sintering. In this case, the temperature sensing resistive element may contain at least one of Mn, Ni, Co, and Fe.

[0018] In an embodiment of the present invention, the temperature sensing resistor film (thermistor) may be formed directly and monolithically onto the carrier sub-

55

strate on which the semiconductor element (e.g., semiconductor laser chip) is mounted.

[0019] Therefore, in the case that the temperature of the semiconductor element transmitted via the carrier substrate is sensed by the temperature sensing resistor film, the thermal resistance between the temperature sensing resistor film and the carrier substrate never changes even after the operation hours of the semiconductor chip have lapsed.

[0020] As a result, the temperature of the laser chip can be controlled without the long term variation that occurs in the prior art and with high precision.

[0021] Reference will now be made, by way of example, to the accompanying drawings, in which:

FIG.1 (described above) is a perspective view showing a previously-proposed semiconductor light emitting device;

FIG.2 to FIG.4 are perspective views showing steps of manufacturing a semiconductor light emitting device according to an embodiment of the present invention; and

FIG.5 is a side view showing the application of the semiconductor light emitting device according to an embodiment of the present invention.

[0022] The steps required to obtain the device shown in FIG.2 will be explained below.

[0023] First, a metal film is formed on a major surface of a ceramic carrier (substrate) 1 formed of ceramics such as alumina, aluminium nitride, etc. This metal film is formed by sputtering sequentially titanium and platinum on the ceramic carrier 1, for example.

[0024] Then, a resist pattern (not shown) of wirings and pads is formed on the metal film, and then the metal film, in regions that are not covered with the resist pattern, is removed by the sputter etching. Thus, an islandlike first conductive pattern 2 is formed at one corner positioned near one end of the major surface of the ceramic carrier 1, and also an L-shaped second conductive pattern 3, on which the laser chip is mounted, is formed at a distance around the first conductive pattern 2. Also, a third conductive pattern 4 and a fourth conductive pattern 5, which extend while bending zigzag along both sides of the ceramic carrier 1, are formed at a distance in the region near the other end of the major surface of the ceramic carrier 1. End portions of the third and fourth conductive patterns 4, 5 positioned near the other end of the ceramic carrier 1 are formed as wirebonding points. Also, bent portions 4a, 5a in the middle of the third and fourth conductive patterns 4, 5 are portions having low thermal conductivity and have a pattern width that is narrower than that of both ends.

[0025] Then, a sintered film that is made of single or composite oxide containing at least one of manganese (Mn), nickel (Ni), cobalt (Co), iron (Fe), etc. is formed directly on the major surface of the ceramic carrier 1 and the first to fourth conductive pattern electrodes 2 to 5 by

sputtering to have a thickness of 0.1 to 2.0  $\mu$ m. Then, the sintered film is burned by heating at several hundreds °C for several hours.

[0026] In turn, as shown in FIG.3, the sintered film is patterned by the photolithography method such that such sintered film remains in regions of the third and fourth conductive patterns 4, 5 that are located on one end portion near the center of the ceramic carrier 1 and between the third and fourth conductive patterns 4, 5. Thus, a thermistor element 6 made of the sintered film (temperature- sensing resistor film) whose both ends are connected to the third and fourth conductive patterns 4, 5 respectively is formed monolithically on the major surface of the ceramic carrier 1. Accordingly, a thermistor carrier having a laser chip mounting region (semiconductor element mounting portion) can be completed.

[0027] Then, as shown in FIG.4, a laser chip 8 is jointed to the second conductive pattern 3 by using a solder 7. In this case, a second electrode 8b of the laser chip 8 is positioned upwardly by jointing a first electrode 8a of the laser chip 8 to the second conductive pattern 3. A heat sink (not shown) may be interposed between the laser chip 8 and the ceramic carrier 1.

[0028] The structure in which the laser chip is fitted on the thermistor carrier is completed through the above steps.

[0029] As shown in FIG.5, the above structure as well as a first lens 11 is fitted onto an insulating substrate 12, and then fixed at such a position that an output end of the laser chip 8 is directed toward the first lens 11. The insulating substrate 12 is fitted onto a Peltier element 20. [0030] Meanwhile, in the structure shown in FIG.4, a first gold wire 13 is bonded to the wire bonding point of the second conductive pattern 3, which is near one end of the ceramic carrier 1, and also is connected to an external laser driving circuit (not shown). Also, a second gold wire 14 is bonded to the second electrode 8b of the laser chip 8 and the first conductive pattern 2, and then a third gold wire 15 is bonded to the first conductive pattern 2 and also is connected to an external laser driving circuit 18.

[0031] In addition, a fourth gold wire 16 and a fifth gold wire 17 are bonded respectively to other end portions of the third and fourth conductive patterns 4, 5, to one end portions of which the thermistor element 6 is connected, and also connected to a differential amplifier 18a of a temperature control circuit 18 shown in FIG.5. That is, the thermistor element 6 is connected to the differential amplifier 18a of the temperature control circuit 18 via the gold wires 16, 17 and the third and fourth conductive patterns 4, 5.

[0032] The differential amplifier 18a can set the temperature of the ceramic carrier 1, i.e., the temperature of the laser chip 8, to a predetermined temperature by comparing the resistance of the thermistor element 6 with a reference resistance value of a reference resistor 18b, then adjusting a current value to the Peltier element

EP 1 229 315 A1

10

20

30

35

40

55

(temperature heating/cooling element) 20 via an amplifier 18c so as to reduce the reference difference to zero, and then controlling the temperature of the Peltier element 20 such that the thermistor element 6 has the reference resistance value. The reference resistance value of the reference resistor 18b is previously set to the resistance value of the thermistor element 6 when the temperature of the laser chip 8 is 25 °C, for example. [0033] In the above optical module, the thermistor element 6 is formed directly and monolithically on the ceramic carrier 1, on which the laser chip 8 is mounted, without intervention from the solder or brazing material whose thermal resistance easily changes. Therefore, the temperature of the laser chip 8 can always be sensed with good precision via the ceramic carrier 1 irrespective of the lapse of the driving time of the laser chip 8, whereby the cooling or heating control of the laser chip 8 made by the temperature control circuit 18 and the Peltier element 20 can be executed with high precision.

[0034] As a result, since the change in microstructure or the progress of cracks due to solder creep does not occur after the laser chip is operated, the temperature of the laser chip 8 fitted onto the ceramic carrier 1 does not vary long term and is kept constant, and thus the optical characteristic of the laser chip 8 can be maintained constant.

[0035] In FIG.5, a reference 21 denotes an optical fiber that is connected optically to the first lens 11 via the second lens 22.

[0036] In the above embodiment, the laser chip (semiconductor laser) is fitted to the semiconductor mounting region on the thermistor carrier. But the temperature of the semiconductor element may be controlled at a constant value by fitting other semiconductor elements onto the semiconductor mounting region.

[0037] As described above, in an embodiment of the present invention, the temperature sensing resistive element is formed directly and monolithically onto the carrier substrate on which the semiconductor chip (e.g., semiconductor laser chip) is mounted. Therefore, in the case that the temperature of the semiconductor chip transmitted via the carrier substrate is sensed by the temperature sensing resistor film, the change in the thermal resistance between the temperature sensing resistor film and the carrier substrate can be prevented even when the operation time of the semiconductor chip becomes longer, so that the temperature of the semiconductor device can be controlled, without the long term variation that occurs in the prior art, and with high precision.

#### Claims

1. A semiconductor device comprising:

a carrier substrate (1);

a temperature sensing resistive element (6) deposited on the carrier substrate (1); a semiconductor element mounting portion (3) laid on the carrier substrate (1); and a semiconductor element (8) mounted on the semiconductor element mounting portion (3).

- 2. A semiconductor device according to claim 1, wherein the carrier substrate (1) is formed of ceramics.
- 3. A semiconductor device according to claim 1 or 2, further comprising conductive patterns (4,5) that are formed on the carrier substrate (1) and connected with the temperature sensing resistive element
- 4. A semiconductor device according to any preceding claim, wherein each of the conductive patterns (4,5) has a bonding point that is electrically connected to an outside (16, 17), and has a portion (4a, 5a) having low thermal conductivity between the bonding point and the temperature sensing resistive element (6).
- 5. A semiconductor device according to any preceding claim, wherein the portion (4a, 5a) having the low thermal conductivity is a bent portion of each of the conductive patterns (4,5).
- A semiconductor device according to any preceding claim, wherein the portion (4a, 5a) having the low thermal conductivity is a small width portion of each of the conductive patterns (4,5).
- 7. A semiconductor device according to any preceding claim, wherein the temperature sensing resistive element (6) contains at least one of Mn, Ni, Co, and Fe.
- A semiconductor device according to any preceding claim, wherein the semiconductor element (8) is a semiconductor laser.
- 45 A semiconductor device according to any preceding claim, wherein a heat sink is interposed between the semiconductor laser (8) and the mounting portion (3).
- 10. A chip carrier comprising:

a carrier substrate (1); a temperature sensing resistive element (6) deposited on the carrier substrate (1); and a semiconductor element mounting portion (3) laid on the carrier substrate (1).

11. A chip carrier according to claim 10, wherein the



carrier substrate (1) is formed of ceramics.

- 12. A chip carrier according to claim 10 or 11, further comprising conductive patterns (4,5) that are formed on the carrier substrate (1) and connected to the temperature sensing resistive element (6).
- 13. A chip carrier according to any one of claims 10 to 12, wherein each of the conductive patterns (4,5) has a bonding point that is electrically connected to an outside (16, 17), and has a portion (4a, 5a) having low thermal conductivity between the bonding point and the temperature sensing resistive element.
- 14. A chip carrier according to any one of claims 10 to 13, wherein the portion (4a, 5a) having the low thermal conductivity is a bent portion of each of the conductive patterns (4,5).
- 15. A chip carrier according to any one of claims 10 to 14, wherein the portion (4a, 5a) having the low thermal conductivity is a small width portion of each of the conductive patterns (4,5).
- 16. A chip carrier according to any one of claims 10 to 15, wherein the temperature sensing resistive element (6) is formed through a step of sintering on the carrier substrate (1).
- 17. A chip carrier according to any one of claims 10 to 16, wherein the temperature sensing resistive element (6) contains at least one of Mn, Ni, Co, and Fe.

10

15

20

--

25

\_\_

30

35

40

45

50

FIG. 1

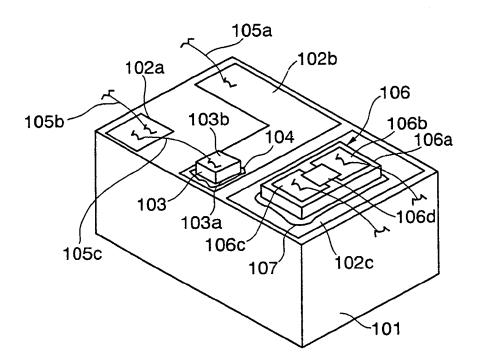


FIG. 2

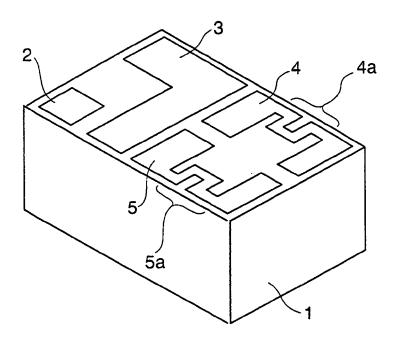


FIG. 3

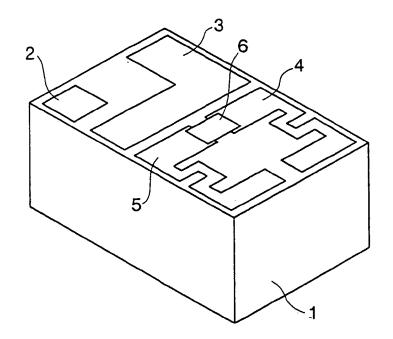
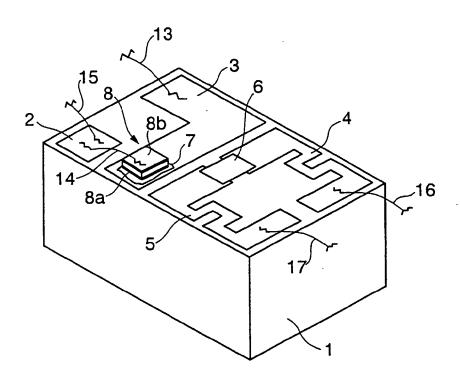


FIG. 4



,22 18c 18b

① REFERENCE RESISTANCE



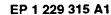
## EP 1 229 315 A1



## **EUROPEAN SEARCH REPORT**

Application Number EP 02 25 0736

Category	Citation of document with indication of relevant passages	, where appropriate,	Relevant to claim	CLASSIFICATION OF THE APPLICATION (INLCI.7)	
D,A	PATENT ABSTRACTS OF JAPA vol. 018, no. 290 (E-155 2 June 1994 (1994-06-02) -& JP 06 061012 A (ISHIZ 4 March 1994 (1994-03-04 * abstract *	7), UKA DENSHI KK),	1,10,16	G01K7/22 H01S5/024	
A	EP 0 467 359 A (FUJITSU 22 January 1992 (1992-01 * the whole document *		1,8,10,		
A	EP 0 259 888 A (NIPPON E 16 March 1988 (1988-03-1 * abstract; figures *		1,9,10		
				TECHNICAL FIELDS SEARCHED (Int.Cl.7)	
				G01K H01S	
	The present search report has been dra	awn up for all claims	7		
	Place of search THE HAGUE	Date of completion of the season 5 April 2002 Rai		Examiner Tiboer, P	
CATEGORY OF CITED DOCUMENTS  X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background		T: theory or princi E: earlier patent of after the filing of D: document ofter L: document ofter	T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons		





# ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

EP 02 25 0736

This annex lists the patent tamily members relating to the parent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is In no way liable for these particulars which are merely given for the purpose of information.

05-04-2002

Patent document cited in search report		Publication date		Patent tamily member(s)	Publication date	
JP	06061012	A	04-03-1994	NONE		
EP	0467359		22-01-1992	JP	3035852 B2	24-04-2000
	0.07003	•••		ĴΡ	4075394 A	10-03-1992
				DE	69104661 D1	1 24-11-1994
				EP	0467359 A2	2 22 <b>-0</b> 1- <b>199</b> 2
				US	5212699 A	18-05-1993
EP	0259888	A	16-03-1988	JP	63070589 A	30-03-1988
	420000	• • •	20 00 000	DE	3788546 DI	1 03-02-1994
				DE	3788546 T2	2 21-04-1994
				EP	0259888 A2	2 16-03-1988
				US	4803689 A	07-02-1989

This Page Blank (uspto)